UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,050	02/05/2004	Fathi M. Salam	6550-62/COB	5452

27572 7590 02/27/2007
HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
COUGHLAN, PETER D	
ART UNIT	PAPER NUMBER
2129	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,050	SALAM ET AL.	
	Examiner	Art Unit	
	Peter Coughlan	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *43-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to an AMENDMENT entered December 21, 2006 for the patent application 10/773050 filed on February 5, 2004.

2. The First Office Action of August 21, 2006 is fully incorporated into this Final Office Action by reference.

Status of Claims

3. Claims 43-90 are pending.

Drawings

4. Claims 44, 63, 84 states that a column represents a neuron of a neural network. The specification states that Figure 1 illustrates a column, which represents a neuron of a neural network (¶0026). The objection with Figure 1 is that there is no defined boundaries or limitations illustrated within Figure 1 which indicate a 'column' or a 'neuron.'

This figure must be corrected or withdrawn from the application.

There is a typographical mistake within the amended claims. The listing of claims state that claims 1-44 are cancelled. The original set of claims only ranged from 1-42.

35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 43-90 are rejected under 35 U.S.C. 101 for nonstatutory subject matter. The computer system must set forth a practical application of that § 101 judicial exception to produce a real-world result. Benson, 409 U.S. at 71-72, 175 USPQ at 676-77. The invention is ineligible because it has not been limited to a substantial practical application. A chip that is 'self programming' for uses in prediction, estimation and control is not a practical application. These are abstract concepts and can fulfill numerous practical applications. The result has to be a practical application. Please see the interim guidelines for examination of patent applications for patent subject matter eligibility published November 22, 2005 in the official gazette.

In determining whether the claim is for a "practical application," the focus is not on whether the steps taken to achieve a particular result are useful, tangible and concrete, but rather that the final result achieved by the claimed invention is "useful, tangible and concrete." If the claim is directed to a practical application of the § 101 judicial exception producing a result tied to the physical world that does not preempt the judicial exception, then the claim meets the statutory requirement of 35 U.S.C. § 101. The phrase 'self-programming, mixed mode chip for estimation, prediction and control', is not clear in its purpose or scope. There has to be some real world purpose or function, which this chip can be used for. Is this to be used for robotic movement in uneven terrain? If so, such results have not been claimed.

The invention must be for a practical application and either:

1) specify transforming (physical thing) or

2) have the FINAL RESULT (not the steps) achieve or produce a

useful (specific, substantial, AND credible),

concrete (substantially repeatable/ non-unpredictable), AND

tangible (real world/ non-abstract) result.

A claim that is so broad that it reads on both statutory and non-statutory subject matter, must be amended, and if the specification discloses a practical application but the claim is broader than the disclosure such that it does not require the practical application, then the claim must be amended.

A claim that recites a chip that self programs itself is nonstatutory. There must be a result that is a practical application.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 49, 68, 89 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. These claims state that a row is equivalent to a neuron of a neural network. The specification makes no such statement.

These claims must be amended or withdrawn from consideration.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 43-57, 59-76, 78-80 are rejected under 35 U.S.C. 102(b) (hereinafter referred to as **Oh**) being anticipated by Oh, 'Analog CMOS Implementation of Artificial Neural Networks for Temporal Signal Learning.'

Claim 43

Oh teaches an array of synaptic cells (Applicant states that Fig. 1 is a 3X3 synaptic cell structure. Oh discloses Figure 6.7 is a 4X5 array.(p127) The 'synaptic cell structure' of applicant is equivalent to 'array' of Oh.) which are interconnected to form a feedforward neural network, wherein each synaptic cell includes(**Oh,** p4:19 through p5:2): a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor(**Oh,** p116:2-17); a digital memory operable to store the local weight in a digital form(**Oh,** p116:2-17; When the analog signal is inputted, it is converted to digital by the AD converter. The values of this process are stored within registers. These registers which contain the results of the AC conversion is equivalent to 'digital memory' of applicant.) Using the digital to analog converter ensures the capacitor is always refreshed, thus indicating the local weights are stored in a digital form.); and a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of an analog input signal in accordance with the local weight stored in the digital memory.(**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claims 44, 63

Oh teaches wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh,** p13:4 through p15:7, Fig 1., equation 2.3; Applicant discloses a 'synaptic cell structure' in the form of 3X3. This 3X3 can be seen as a matrix. It follows that the computational requirements of multiplying each 'i' input values with each 'j' weight value and the summation for each 'i' follows matrix multiplication illustrated in equation 2.3. Thus each neuron's result is equal to y_i . The neuron which is a 'column' of applicant is equivalent to the row w_{iM} of Oh.)

Claims 45, 64

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells. (**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.)

Claims 46, 65

Oh teaches wherein the control cells operate synchronously with each other to control conversion. (**Oh,** p12:14 through p13:3; Oh discloses in the McCulloch-Pitts model, in which neurons operate in asynchronous manner. Using Oh's model in which the feedfordward neural network is interconnected allows synchronously operations to occur.)

Claims 47, 66

Oh teaches wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells (**Oh,** figure 6.2; Figure 6.2 illustrates numerous multiplexers within the recurrent neural network.) and an analog-to-digital converter. (**Oh,** p116:2-17)

Claims 48, 67

Oh teaches wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells. (**Oh,** p116:2-17)

Claims 49, 68

Oh teaches wherein each row of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh,** Figure 6.2; Each row of Figure 6.2 represents a 'neuron' due to the fact there is a 'sigmoid' associated with each row. The 'sigmoid' determines if the 'neuron' fires or not, which parallels a 'neuron'.)

Claims 50, 69

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a column of synaptic cells in the array of synaptic cells. (**Oh,**

p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.)

Claims 51, 70

Oh teaches a switch interposed between the processing circuit and the digital memory for selectively enabling use of the digital memory. (**Oh,** p116:2-17; Oh discloses a second recurrent neural network (slave neural network) which employs the weight values from the first recurrent neural network. These values are updated using the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claims 52, 71

Oh teaches a switch interposed between the processing circuit and the learning circuit for selectively enabling use of the learning circuit. (**Oh,** p116:2-17; Oh discloses a first recurrent neural network (master neural network) which employs the learning phase of the neural network or learning circuit of applicant. These values are updated using the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claims 53, 72

Oh teaches a switch interposed between the processing circuit, the learning circuit and the digital memory for selectively enabling the use of either the learning

circuit or the digital memory by the processing circuit. (**Oh,** p116, 2-17; If there exists two phases, a learning phase and a testing phase, then there exists a switch to alter between the two phases.)

Claims 54, 73

Oh teaches the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule. (**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claims 55, 74

Oh teaches the learning circuit is configured to receive an error signal indicative of a difference between an output signal and a target output signal. (**Oh,** p15:9 through p16:7; 'Output signal' and 'target output signal' of applicant is equivalent to 'actual output' and 'desired output' of Oh.)

Claims 56, 73

Oh teaches multiple arrays of synaptic cells which are interconnected to form a multi-layer neural network. (**Oh,** figure 6.2; Figure 6.2; The 2 dimensional array which each node is interconnected with other nodes of Oh is equivalent to 'multi-layer neural network' of applicant.)

Claims 57, 76

Oh teaches the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network.(**Oh,** p17:5-6 and equation (2.11); 'Error signal' of applicant is equivalent to 'w^{k}' of Oh. 'Previous layer' of applicant is equivalent to 'w^{k-1}' of Oh.)

Claims 59, 78

Oh teaches a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell. (**Oh,** p116:2-17; Oh discloses a digital to analog converter for outputting the value of the synaptic cell.)

Claims 60, 79

Oh teaches wherein each processing circuit in a column of synaptic cells outputs a component of a weighted sum.(**Oh,** p13:4 through p15:8; 'Processing circuit in a column' of applicant is equivalent to 'the 'hidden layer' of Oh. 'Outputs a component of a weighted sum' of applicant is equivalent to the output of each node in the hidden layer is a result of the weighted sum input.)

Claims 61, 80

Oh teaches wherein an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum. (**Oh,** figure 5.5; Oh discloses the output of each multiplier (Y_1-Y_4) is fed back as a column to form a interconnection of synaptic cells.)

Claim 62

Oh teaches an array of synaptic cells which are interconnected to form a feedforward neural network(**Oh,** p4:19 through p5:2)and configured to receive an analog input signal indicative of a biological cell measurement and to model a process of the biological cell, wherein each synaptic cell includes (**Oh,** p3:6-10; 'Configured to receive ... analog input' of applicant is disclosed by a 'subthreshold analog CMOS VLSI' of Oh.) a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor(**Oh,** p116:2-17; Oh discloses a 'master neural network' which generates weights while in the 'learning phase.' 'Learning electrical circuit' of applicant is equivalent to 'learning phase' of Oh.) a digital memory operable to store the local weight in a digital form (**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.); and a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of the analog input signal in accordance with the local weight stored in the digital memory. (**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 58, 77, 81-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh as set forth above, in view of Newton. ('Newton's Telecom Dictionary', referred to as **Newton**)

Claims 58, 77

Oh does not teach wherein the digital memory is implemented using flip-flops.

Newton teaches wherein the digital memory is implemented using flip-flops.(**Newton,** p316, C2:43-45; It is common knowledge that a flip flop circuit is used to hold digital information.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Oh by disclosing the flip flop circuit as taught by Newton to have the digital memory is implemented using flip-flops.

For the purpose of using industrial standard technology for containing digital values.

Claim 81

Oh teaches an array of synaptic cells which are interconnected to form a feedforward neural network(**Oh,** p4:19 through p5:2), wherein each synaptic cell includes: a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor(**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form and then the digital form is used to refresh a capacitor which contains the 'weight value.'), wherein the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule(**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.), and is configured to receive an error signal indicative of a difference between an output signal and a target output signal (**Oh,** p15:9 through p16:7; 'Output signal' and 'target output signal' of applicant is equivalent to 'actual output' and 'desired output' of Oh.); a digital memory operable to store the local weight in a digital form. (**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.)

Oh does not teach wherein the digital memory is implemented using flip-flops.

Newton teaches wherein the digital memory is implemented using flip-flops.(**Newton,** p316, C2:43-45; It is common knowledge that a flip flop circuit is used to hold digital information.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Oh by disclosing the flip flop circuit as taught by Newton to have the digital memory is implemented using flip-flops.

For the purpose of using industrial standard technology for containing digital values.

Oh teaches a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of an analog input signal in accordance with the local weight stored in the digital memory (**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.) a switch interposed between the processing circuit, the learning circuit, and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit(**Oh,** p116, 2-17; If there exists two phases, a learning phase and a testing phase, then there exists a switch to alter between the two phases.); a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell. (**Oh,** p116:2-17)

Claim 82

Oh teaches multiple arrays of synaptic cells which are interconnected to form a multi-layer neural network (**Oh,** figure 6.2; Figure 6.2; The 2 dimensional array which each node is interconnected with other nodes of Oh is equivalent to 'multi-layer neural network' of applicant.), wherein the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network. (**Oh,** p17:5-6 and equation (2.11); 'Error signal' of applicant is equivalent to 'w^{k}' of Oh. 'Previous layer' of applicant is equivalent to 'w^{k-1}' of Oh.)

Claim 83

Oh teaches an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum, and each processing circuit in a column of synaptic cells outputs a component of the weighted sum. (**Oh,** figure 5.5; Oh discloses the output of each multiplier (Y_1-Y_4) is a result of the summation of weights for a given row. The output of each multiplier is returned into the interconnected array as a column.)

Claim 84

Oh teaches wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh,** Figure 6.2; One function of a neuron is to use it's output for training to convergence. The column(s) of Figure 6.2 illustrate this by using the outcome of 'error' circuit for training purposes.)

Claim 85

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells. (**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.)

Claim 86

Oh teaches wherein the control cells operate synchronously with each other to control conversion. (**Oh,** p12:14 through p13:3; Oh discloses in the McCulloch-Pitts model, in which neurons operate in asynchronous manner. Using Oh's model in which the feedfordward neural network is interconnected allows synchronously operations to occur.)

Claim 87

Oh teaches wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells (**Oh,** figure 6.2; Figure 6.2 illustrates numerous multiplexers within the recurrent neural network.) and an analog-to-digital converter. (**Oh,** p116:2-17)

Claim 88

Oh teaches wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells. (**Oh,** p116:2-17)

Claim 89

Oh teaches wherein each row of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh,** Figure 6.2; Each row of Figure 6.2

represents a 'neuron' due to the fact there is a 'sigmoid' associated with each row. The 'sigmoid' determines if the 'neuron' fires or not, which parallels a 'neuron'.)

Claim 90

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a column of synaptic cells in the array of synaptic cells. (**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.)

Response to Arguments

5. Applicant's arguments filed on December 21, 2006 for claims 43-90 have been fully considered but are not persuasive.

6. In reference to the Applicant's argument:

Claims 43-89 are now pending in the application. Claims 1-42 are cancelled. Claims 43-89 are added. Support for the additions can be found throughout the originally filed specification, and especially at Figures 1, 2, and 7 and related discussion. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

STATEMENT OF THE SUBSTANCE OF THE INTERVIEW

Applicants thank the Examiner for the telephonic interview with Applicants' representatives on December 8, 2006. Therein, new claims were discussed, particularly with reference to Figure 2. Agreement was not reached.

SPECIFICATION

The specification stands objected to for certain informalities. These objections are respectfully traversed.

Applicants respectfully submit that these objections are rendered moot by cancellation of claims 1-42 herein.

Therefore, reconsideration and withdrawal of these objections is respectfully requested.

REJECTION UNDER 35 U.S.C. § 101

Claims 1-42 stand rejected under 35 U.S.C. § 101 for non-statutory subject matter. This rejection is respectfully traversed.

Applicants respectfully submit that these rejections are rendered moot by cancellation of claims 1-42 herein. Moreover, with regard to rejection under 35 U.S.C. § 101, Applicant has reviewed the interim guidelines for examination. The proposed claim recites an architecture for a chip which includes different electric circuits having multipliers and capacitors as well as a digital memory. This recited subject matter clearly falls within the category of a machine and outside the enumerated judicial exceptions.

Accordingly, Applicants respectfully request the Examiner reconsider and withdraw the rejection of the claims under 35 U.S.C. § 101.

Examiner's response:

The Examiner acknowledges the withdraw of claims 1-42. Claims 43-90 are still

rejected under 35 U.S.C. §101.

7. In reference to the Applicant's argument:

REJECTION UNDER 35 U.S.C. § 102

Claims 1-4, 8-14, 17-19, 23, 25, 26, 28-34, 36, 38, 39, 41, and 42 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Winder (U.S. Pat. No. 6,213,958). This rejection is respectfully traversed.

Applicants respectfully submit that this rejection is rendered moot by cancellation of claims 1-42 herein.

Accordingly, Applicants respectfully request the Examiner reconsider and withdraw the rejections of claims 1-4, 8-14, 17-19, 23, 25, 26, 28-34, 36, 38, 39, 41, and 42 under 35 U.S.C. § 102(e).

Examiner's response:

The reference 'Oh' anticipates all the new claims except 58, 77 and 81.

8. In reference to the Applicant's argument:

REJECTION UNDER 35 U.S.C. § 103

Claims 5, 6, 16, 22, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Winder (U.S. Pat. No. 6,213,958) in view of Salam (U.S. Pat. No. 5,689,621). This rejection is respectfully traversed.

Applicants respectfully submit that this rejection is rendered moot by cancellation of claims 1-42 herein.

Accordingly, Applicants respectfully request the Examiner reconsider and withdraw the rejection of claims 5, 6, 16, 22, and 35 under 35 U.S.C. § 103(a).

Claims 7, 15, 20, 21, 24, and 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Winder (U.S. Pat. No. 6,213,958) in view of Thaler (U.S. Pat. No. 6,014,653). This rejection is respectfully traversed.

Applicants respectfully submit that this rejection is rendered moot by cancellation of claims 1-42 herein.

Accordingly, Applicants respectfully request the Examiner reconsider and withdraw the rejection of claims 7, 15, 20, 21, 24, and 37 under 35 U.S.C. § 103(a).

Claim 27 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Winder (U.S. Pat. No. 6,213,958) in view of Greenberger (U.S. Pat. No. 6,675,187). This rejection is respectfully traversed.

Applicants respectfully submit that this rejection is rendered moot by cancellation of claims 1-42 herein.

Accordingly, Applicants respectfully request the Examiner reconsider and withdraw the rejection of claims 27 under 35 U.S.C. § 103(a).

Claim 40 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Winder (U.S. Pat. No. 6,213,958) in view of Thaler (U.S. Pat. No. 6,014,653) and Salam (U.S. Pat. No. 5,689,621). This rejection is respectfully traversed.

Applicants respectfully submit that this rejection is rendered moot by cancellation of claims 1-42 herein.

Accordingly, Applicants respectfully request the Examiner reconsider and withdraw the rejections of claim 40 under 35 U.S.C. § 103(a).

Examiner's response:

The reference art 'Newton' in combination with 'Oh' anticipates claims 58, 77 and 81.

9. In reference to the Applicant's argument:

NEW CLAIMS 43-90

New independent claim 43, recites, "A self-programming, mixed-mode chip for estimation, prediction and control, comprising: an array of synaptic cells which are interconnected to form a feedforward neural network, wherein each synaptic cell includes: a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor; a digital memory operable to store the local weight in a digital form; and a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of an analog input signal in accordance with the local weight stored in the digital memory."

Of note, Applicant's claimed architecture stores weights for each cell locally in a capacitor and locally in a digital memory. New independent claims 62 and 81 recite similar subject matter. The prior art references cited by the Examiner do not teach, suggest, or motivate the claimed subject matter, including this noted feature. These differences are significant. Therefore, new claims 43-90 should be in condition for allowance.

Examiner's response:

The new claims are rejected under 35 U.S.C. ¶101, 102(b) and 103.

Examination Considerations

10. The claims and only the claims form the metes and bounds of the invention. "Office personnel are to give the claims their broadest reasonable interpretation in light of the supporting disclosure. *In re Morris*, 127 F.3d 1048, 1054-55, 44USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d, 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)" (MPEP p 2100-8, c 2, l 45-48; p 2100-9, c 1, l 1-4). The Examiner has the full latitude to interpret each claim in the broadest reasonable sense. Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

11. Examiner's Notes are provided to assist the applicant to better understand the nature of the prior art, application of such prior art and, as appropriate, to further

indicate other prior art that maybe applied in other office actions. Such comments are entirely consistent with the intent and sprit of compact prosecution. However, and unless otherwise stated, the Examiner's Notes are not prior art but link to prior art that one of ordinary skill in the art would find inherently appropriate.

12. Examiner's Opinion: Paragraphs 10 and 11 apply. The Examiner has full latitude to interpret each claim in the broadest reasonable sense.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Claims 43-90 are rejected.

Correspondence Information

15. Any inquiry concerning this information or related to the subject disclosure should be directed to the Examiner Peter Coughlan, whose telephone number is (571) 272-5990. The Examiner can be reached on Monday through Friday from 7:15 a.m. to 3:45 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor David Vincent can be reached at (571) 272-3080. Any response to this office action should be mailed to:

Commissioner of Patents and Trademarks,

Washington, D. C. 20231;

Hand delivered to:

Receptionist,

Customer Service Window,

Randolph Building,

401 Dulany Street,

Alexandria, Virginia 22313,

(located on the first floor of the south side of the Randolph Building);

or faxed to:

(571) 272-3150 (for formal communications intended for entry.)

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Peter Coughlan

2/21/2007

JOSEPH P HIRL
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100